UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/478,122	01/05/2000	Laurence A. Thompson	DVDOP015	1276

7590 04/08/2004

PERKINS COLE LLP
101 JEFFERSON DRIVE
MENLO PARK, CA 94025-1114

EXAMINER	
LAO, LUN S	

ART UNIT	PAPER NUMBER
2643	

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/478,122	THOMPSON, LAURENCE A.	
	Examiner	Art Unit	
	Lun-See Lao	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This action is response to the amendment filed on 1-23-2004. Claims 1,2,8,10,13,15-18,20-22, 25, 26-28 and 31 have been amended, claim 35 has been added. Claims 1-35 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1–9, 20-27 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US PAT 6,272,153) in view of Applicant's prior art.

Consider claim 1, Huang teaches an input device (see fig.5 (502,504)) receptive to a digital audio signal and operative to detect (510,512) a format of the digital audio signal and provide a format signal (such as MPEG audio or AC3 audio format); and

a processing device (508) coupled to the input device (504,502) to receive the digital audio signal and the format signal, the processing device (508) configured for providing a time in the digital audio signal the duration (see fig.5, 516 (output)) of which is related to the detected format (such as MPEG audio and AC3 audio) of the digital audio signal

(see col.7 line 24-col.8 line 43), but Huand does not clearly teach to provide a time delay.

However, Applicant's prior art teaches a providing of time delay (see fig.1 and specification pages 2-3).

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Huang into applicant's prior art to provide to synchronize the audio and video signal is depend upon the format of the video and corresponding audio signal of umber of formats are used for digital video signal.

As to claim 20, there is the method claim corresponding to apparatus claim 1, see previous apparatus claim 1 rejection.

Consider claims 2-3, Huang teaches the apparatus of the digital audio signal further comprises inherently a serial audio clock signal (to synchronize an audio signal output from the internal decoder and an audio signal out put from the external, it needs a clock cycle to control it) and a plurality of accompanying signals (see col.2 line 25- 67); and the accompanying signals further comprises a data signal and a frame synchronization signal (see col.2 lines 25-67).

As to claims 21 and 23, these are the method claims of claims 2-3 respectively. Thus note claims 2-3, respectively for rejection.

Consider claims 4-7, Huang teaches the apparatus of the accompanying signals are loaded into a register (see fig.5, (508)); and the register is a FIFO register (col.9 lines 15-41); and the accompanying signals are stored in a memory device (see fig.5 (528

and 532)); and the memory device further comprises a memory controller (DSP) and a memory chip (DRAM and see col.5 line 13 –col.6 line56).

As to claims 24-25, these are the method claims of claims 6-7 respectively. Thus note claims 6-7, respectively for rejection.

Consider claim 35, Applicant's prior art teaches that the apparatus comprising an output device (see fig.1 output), coupled to the processing device (provide delay X,Y, Z), to output the audio signal with delay corresponding to the format of the audio signal (see specification page 2-3)

Consider claims 8-9, Huang teaches the apparatus of the processing device (see fig.5, 508) further comprises an audio format detection device operable to detect the format of the digital audio signal (see col.30-col.8 line 58) and the apparatus of the audio format detection device (see fig.5, (508)) is operable to detect a number of edge (by state machines) transitions in the serial audio clock signal (see col.7 line 30-col.8 line 58).

As to claims 26-27, these are the method claims of claims 8-9 respectively. Thus note claims 8-9, respectively for rejection.

4. Claims 10-14, 17-18, 22 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US PAT. 6,272,153) as modified by Applicant's prior art as applied to claims 1-7 and 20-21 above, and further in view of Kuwaoka (US PAT. 6,449,519).

Consider claim 10, Huang and applicant's prior art do not clearly teaches

the apparatus of the audio format detection device further comprises a plurality of model data, wherein each model data represents one of a plurality of audio signal formats and a corresponding one of a plurality of time delay data, wherein the detected count is compared to the model data, the audio format detection device operable to provide the delay data representing the model data that is equal to the detected count.

However, Kuwaoka teaches the apparatus of the audio format (formation) detection device (28,25i) further comprises a plurality of model data (25-25h), wherein each model data represents one of a plurality of audio signal formats (formations) and a corresponding one of a plurality of time delay data, wherein the detected count (28,25i) is compared (23,24) to the model data, the audio format (formation) detection device (25i,28) operable to provide the delay data representing the model data that is equal to the detected count (see col.8 line 28-col.9 line 50).

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Huang and applicant's prior art into the teaching of Kuwaoka to provide a compact and high-performance audio information processing apparatus.

As to claim 28, there is the method claim corresponding to apparatus claim 10, see previous apparatus claim 10 rejection.

Consider claim 11 Huang teaches the apparatus of the processed clock signal is synchronized inherently to a reference clock (see col.6 line 40-col.7 line 65).

Consider claim 12 Huang teaches the apparatus of the audio format (frame data) detection device is inherently operable to provide a processed clock signal by dividing the serial audio clock signal by a constant (see col.4 line 14-65).

Consider claim 22, there is the method claim corresponding to apparatus claim 12, See previous apparatus claim 12 rejection.

Consider claims 13-14 and 17-18, Kuwaoka teaches the apparatus of the processing device is operable to compare a new time delay data (current audio data) to an old time delay data (audio data of a before), the processing device operable to reconfigure a buffer if the new time delay data is not equal to the old time delay data (see col.9 line 17-35); and the apparatus of the detected count is compared to the model data by a plurality of comparators (see fig.3, (23,24) and col.9 line 17-57); and the apparatus of the processing device further comprises a memory unit (see fig.3, 25) to provide the time delay corresponding to the time delay data (see col.8 lines 27-65); and the apparatus of the processing device further comprises a first parameter and a second parameter, the first parameter configured according to the provided time delay data.

Consider claim 29, there is the method claim corresponding to apparatus claim 14, See previous apparatus claim 14 rejection.

Consider claim 17, Applicant's prior art teaches the apparatus of the processing device further comprises a memory unit to provide the time delay (see fig.1, provide delay of X, Y, Z) corresponding to the time delay data (see specification pages 2-3);

5. Claims 15-16, 18-19, 22 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US PAT. 6,272,153) as modified by Applicant's prior art and Kuwaoka (US PAT. 6,449,519) as applied to claims 1-12 and 20-28 above, and further in view of Sueyoshi et al (US PAT. 6,233,562).

Consider claim 15, Huang, applicant's prior art and Kuwaoka do not teach the apparatus of the provided time delay data is a first offset value, the processing device operable to resize a write address pointer with the offset value.

However Sueyoshi teaches the apparatus of the provided time delay data is a first offset value (see fig.1 4a, sent by pointer controller), the processing device operable to resize a write address pointer (actual pointer and temporary pointer) with the offset value (sent by pointer controller, 4a and see col.4 lines 2-42);

Therefore, it would obvious to one of ordinary skill in the art at the time invention was made to combine the teaching of Huang, Kuwaoka and applicant's prior art into the teaching of Sueyoshi for reducing the required capacity of the buffer memory provided there between while synchronizing the audio signal out from the internal decoder and the audio signal output from the external decoder.

Consider claim 16 Sueyoshi teaches the apparatus of the provided time delay data is a second offset value (sent by pointer controller, 4a), the processing device operable to resize a read address pointer (actual pointer and temporary pointer) with the offset value (sent by pointer controller, 4a and see col.4 lines 2-42).

Consider claims 18-19, Sueyoshi teaches apparatus of the processing device (see fig.1, 2) further comprises a first parameter (write = replace information) and a second

parameter (read information), the first parameter configured inherently according to the provided time delay data (see col.4 lines 2-44); and the apparatus of the first parameter (information) is a write address parameter (actual pointer and temporary pointer), the second parameter (information) is a read address parameter (actual pointer and temporary pointer), and the memory unit is a buffer (see col.4 lines 2-44).

Consider claim 22, Sueyoshi teaches the method of the step of processing the digital audio signal further comprises the step of providing inherently a processed serial audio clock signal, the processed serial audio clock signal provided by dividing the serial audio clock signal (such as each frame fk (k=1,2, 3.... Constant) by a constant (see col.13 line 60-col.14 line4).

Consider claims 30-31, Sueyoshi teaches the method of the detected count further comprises the number of edge (border) transitions in the processed inherently serial audio clock signal within a period (each frames), and wherein the plurality of model data include the number of edge (border) transitions present in each processed serial audio clock signal format in the period (each frames and see col.13 line 60-col.14 line 43) and the method of the step of processing the digital audio signal further comprises the step of providing a memory register (see fig.1, (1,2,,3) having a first parameter (actual pointer for replace information) and a second parameter (actual pointer for reading information), the memory register inherently configured to provide a delay (see col.4 lines 3-43).

Consider claims 32-34, Sueyoshi teaches the method of the step of providing a memory register (see fig.1, (1,2, 3)) further comprises the step of providing an offset (

4a, pointer controller), the offset corresponding to inherently the model data equal to the detected count and resizing the memory register by providing the offset (pointer controller) for the first parameter (replaced with information)(see col.4 lines 2-44); and the method of the first parameter (replaced with information) is a write address pointer(actual pointer and temporary pointer), the second parameter (reading information) is a read address pointer (actual pointer and temporary pointer), and the memory register is a buffer (see col.4 lines 2-42); the method of the first parameter (reading information) is a read address pointer(actual pointer and temporary pointer), the second parameter (replaced with information) is a write address pointer(actual pointer and temporary pointer), and the memory register is a buffer (see col.4 lines 2-42).

Response to Arguments

6. Applicant's arguments with respect to claim1-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art of record and not relied upon is considered pertinent to applicant's disclosure. Huang et al (US PAT 6,119,091) is recited to show other related the audio signal delay apparatus and method.

9. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (703) 305-2259 The examiner can normally be reached on Monday-Friday from 8:00 to 6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz, can be reached on (703) 305-4708.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (703) 306-0377.

Lao,Lun-See
Patent Examiner
US Patent and Trademark Office
Crystal Park 2
(703305-2259

DUC NGUYEN
PRIMARY EXAMINER